



138.0001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pechanek

Serial No.: 10/648,154

Filed: August 26, 2003

For: METHODS AND APPARATUS FOR  
META-ARCHITECTURE DEFINED  
PROGRAMMABLE INSTRUCTION  
FETCH FUNCTIONS SUPPORTING  
ASSEMBLED VARIABLE LENGTH  
INSTRUCTION PROCESSORS

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date set forth below:

Signed: 

Name: Karen S. Flynn

Date: October 30, 2003

Group: Not Yet Assigned

Examiner: Not Yet Assigned

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Durham, North Carolina  
October 30, 2003

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER § 197(a)

Sir:

This Information Disclosure Statement is being filed before a first Official Action has been mailed in this case.

Pursuant to 37 C.F.R. 1.56, 1.97 and 1.98, applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following items listed on the accompanying Form PTO/SB/08B.

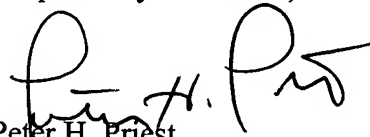
## ITEMS

### Other Publications

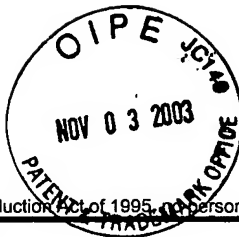
1. BLAUUW ET AL., Computer Architecture: Concepts and Evolution, 1997, Page(s) 71-75, 589-590, 648-664, Publisher: Addison-Wesley, Published in: Reading, Mass.
2. JOHNSON, An Introduction to Vector Processing, Computer Design, February 1978, Page(s) 89-97
3. PECHANNEK ET AL., The ManArray Embedded Processor Architecture, Proceedings of the 26th EUROMICRO Conference, 2000, Page(s) 348-355, Publisher: IEEE Computer Society
4. PELEG ET AL., Intel MMX for Multimedia PCs, Communications of the ACM, January 1997, Page(s) 25-38, Volume 40, Number 1

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made nor shall it be construed as an admission that the information cited is considered to be material to patentability, nor shall it be construed that no other material information exists.

Respectfully submitted,



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PTO/SB/08B (06-03)

Approved for use through 06/30/2003. OMB 0651-0031  
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<b>Substitute for form 1449B/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/648,154
				Filing Date	08/26/2003
				First Named Inventor	Pechanek
				Art Unit	
Sheet	1	of	1	Examiner Name	
				Attorney Docket Number	138.0001

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		BLAUW ET AL., Computer Architecture: Concepts and Evolution, 1997, Page(s) 71-75, 589-590, 648-664, Publisher: Addison-Wesley, Published in: Reading, Mass.	
		JOHNSON, An Introduction to Vector Processing, Computer Design, February 1978, Page(s) 89-97	
		PECHANKE ET AL., The ManArray Embedded Processor Architecture, Proceedings of the 26th EUROMICRO Conference, 2000, Page(s) 348-355, Publisher: IEEE Computer Society	
		PELEG ET AL., Intel MMX for Multimedia PCs, Communications of the ACM, January 1997, Page(s) 25-38, Volume 40, Number 1	

Examiner Signature	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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